substrate.

5. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge circuit further comprises a fifth doping region having said second conductivity type, disposed at the conjunction of said well region and said substrate, for reducing the breakdown voltage at the conjunction of said well region and said substrate.

7. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises a MOS transistor having a first conductivity type disposed on said substrate and comprising a gate and two source/drain regions, wherein one of said source/drain regions is electrically coupled to said well region, while the other of said source/drain regions, together with said gate, is electrically coupled to said reference potential.

8. (Amended) The electrostatic discharge protection circuit as claimed in claim 7, wherein one of said drain/source regions of said MOS transistor having said first conductivity type is comprised of said fifth doping region, and the other of said drain/source regions of said MOS transistor having said first conductivity type is comprised of said second doping region.

9. (Amended) The electrostatic discharge protection circuit as claimed in claim 7, wherein one of said drain/source regions of said MOS transistor having said first conductivity type is comprised of said fifth doping region, and the other of said drain/source regions of said MOS transistor having said first conductivity type is comprised of said second doping region.

10. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises:

a MOS transistor having said first conductivity type, formed on said substrate, comprising a gate, and two source/drain regions, wherein one source/drain region is electrically coupled to said well region, and the other source/drain region is electrically coupled to said reference potential;

a resistor, its two ends electrically coupled to said gate and said reference potential, respectively; and

a capacitor, its two ends electrically coupled to said gate and said node, respectively.

A3 Cont.

11. (Amended) An electrostatic discharge protection circuit with high trigger current, coupled to a node and a reference potential, for dissipating the electrostatic discharge current from said node, comprising:

a BJT, comprising an emitter, a base and a collector, wherein said emitter and said base are electrically coupled to said reference potential, said collector is comprised of a collector region with a second conductivity type and electrically coupled to said node; and

a first doping region having a first conductivity type, electrically floated in said collector region, and forms a conjunction interface with said collector region;

wherein said first doping region, when said electrostatic discharge current is greater than a predetermined current, reduces the potential difference between said node and said reference potential.

12. (Amended) The electrostatic discharge protection circuit as claimed in claim 11, wherein said electrostatic discharge protection circuit

further comprises a MOS transistor having a first conductivity type, disposed on said substrate, comprising a gate, and two source/drain regions, wherein one of said source/drain regions is electrically coupled to said collector, while the other source/drain region, together with said gate, is electrically coupled to said reference potential.

A3 end

13. (Amended) The electrostatic discharge protection circuit as claimed in claim 11, wherein said electrostatic discharge protection circuit further comprises:

a MOS transistor having said first conductivity type, comprising a gate, and two source/drain regions, wherein, one source/drain regions is electrically coupled to said node, and the other source/drain is electrically coupled to said reference potential;

a resistor, its two ends electrically coupled to said gate and said reference potential, respectively; and

a capacitor, its two ends electrically coupled to said gate and said node, respectively.

19. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge protection circuit further comprises a fourth doping region having said first conductivity type, disposed at the surface of said base near said well region, electrically coupled to said reference potential, for forming an ohmic connection at said base.

A4

20. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge circuit further comprises a fifth doping region having said second conductivity type,

disposed at the conjunction of said well region and said base, for reducing the breakdown voltage at the conjunction of said well region and said base.

21. (Amended) The electrostatic discharge protection circuit as claimed in claim 20, wherein said electrostatic discharge protection circuit further comprises a field oxide layer, disposed at the surface of said base adjacent to said fifth doping region.

A4 end

22. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge protection circuit further comprises a MOS transistor having a first conductivity type, disposed on said base, comprising a gate, and two source/drain regions, wherein, one of said source/drain regions is coupled to said well region, while the other source/drain region, together with said gate, is coupled to said reference potential.

Please cancel claim 23 without prejudice.

24. (Amended) The electrostatic discharge protection circuit as claimed in claim 22, wherein, one of said drain/source regions of said MOS transistor having said first conductivity type is comprised of said fifth doping region, and the other drain/source regions of said MOS resistor having said first conductivity type is comprised of said second doping region.

A5

25. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises:

a MOS transistor having said first conductivity type, formed on said

base, and comprising a gate and two source/drain regions, wherein one source/drain region is coupled to said well region, and the other source/drain region is coupled to said reference potential;

a resistor, its two ends coupled to said gate and said reference potential, respectively; and

a capacitor, its two ends coupled to said gate and said node, respectively.

26. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge circuit further comprises a sixth doping region having said first conductivity type, disposed at the conjunction of said well region and said base, for reducing the breakdown voltage at the conjunction of said well region and said base.

28. (Amended) The electrostatic discharge protection circuit as claimed in claim 27, wherein said electrostatic discharge protection circuit further comprises a MOS transistor having a second conductivity type, disposed on said well region, comprising a gate and two source/drain regions, wherein one of said source/drain regions is electrically coupled to said base, while the other source/drain region, together with said gate, is electrically coupled to said node.

29. (Amended) The electrostatic discharge protection circuit as claimed in claim 28, wherein, one of said drain/source of said MOS resistor having said second conductivity type is comprised of said sixth doping region, and the other drain/source of said MOS resistor is comprised of said third doping region.

30. (Amended) The electrostatic discharge protection circuit as claimed in claim 28, wherein, one of said drain/source of said MOS transistor having said second conductivity type is comprised of said sixth doping region, and the other drain/source of said MOS transistor is comprised of said third doping region.

31. (Amended) The electrostatic discharge protection circuit as claimed in claim 26, wherein said electrostatic discharge protection circuit further comprises:

a MOS transistor having said second conductivity type, comprising a gate, and two source/drain regions, wherein, one source/drain region is electrically coupled to said node, and the other source/drain region is electrically coupled to said reference potential;

a resistor, its two ends electrically coupled to said gate and said node, respectively; and

a capacitor, its two ends electrically coupled to said gate and said reference voltage, respectively.

34. (Amended) An electrostatic discharge protection circuit with high trigger current, electrically coupled to a node and a reference potential for dissipating the electrostatic voltage formed at said node, said electrostatic discharge protection circuit comprising:

a BJT, comprising an emitter, a base and a collector, wherein said emitter and said base are electrically coupled to said node, said collector is comprised of a collector region with a first conductivity type and electrically coupled to said reference potential; and

a second doping region having a second conductivity type, electrically floated in said collector region, and forms a conjunction interface with said

collector region;

wherein said second doping region, when said electrostatic discharge current is greater than a predetermined current, reduces the potential difference between said node and said reference potential.

35. (Amended) The electrostatic discharge protection circuit as claimed in claim 34, wherein said electrostatic discharge protection circuit further comprises a MOS transistor having a first conductivity type, comprising a gate, and two source/drain, wherein, one of said source/drain is electrically coupled to said collector, while the other source/drain region, together with said gate are electrically coupled to said reference potential.

36. (Amended) The electrostatic discharge protection circuit as claimed in claim 34, wherein said electrostatic discharge protection circuit further comprises:

a MOS transistor having said first conductivity type, comprising a gate, and two source/drain, wherein, one source/drain is electrically coupled to said node, and the other source/drain is electrically coupled to said reference potential;

a resistor, its two ends are respectively electrically coupled to said gate and said reference potential; and

a capacitor, its two ends are respectively electrically coupled to said gate and said node.

REMARKS

This response amends claims 3, 5, 7-13, 19-22, 24-26, 28-31, and 34-